ABSTRACT OF THE DISCLOSURE

A dynamic logic return-to-zero (RTZ) latching mechanism including a complementary pair of evaluation devices responsive to a clock signal, a dynamic evaluator, delayed inversion logic, and latching logic. The dynamic evaluator is coupled between the complementary pair of evaluation devices at a pre-charged node and evaluates a logic function based on at least one input data signal. The latching logic asserts the logic state of an output node based on the state of the pre-charged node during an evaluation period between an operative edge of the clock signal and the next edge of an evaluation complete signal, which is a delayed and inverted version of the clock signal. The output node is returned to zero between evaluation periods. A footless latching domino circuit may be added to convert the RTZ output to a registered output signal.